Abstract of Disclosure

A unit cell included in a non-volatile dynamic random access memory (NVDRAM) includes a control gate layer coupled to a word line; a capacitor for storing data; a floating transistor for transmitting stored data in the capacitor to a bit line, gate of the floating transistor being a single layer and serving as a temporary data storage; and a first insulating layer between the control gate layer and the gate of the floating transistor, wherein a voltage supplied to body of the floating transistor is controllable.